



IPC/IMEC/ESA Microvia TV HATS² Test Results

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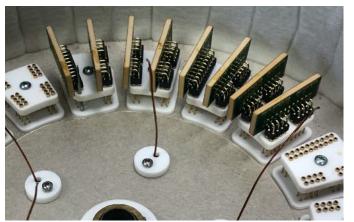


Technical Conference March 9–12, 2021



Introduction to HATS² Testing Technology

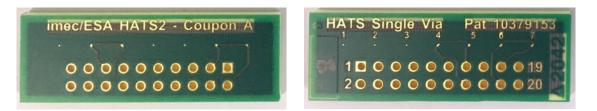
- The HATS^{2™} Tester Can Perform Reflow Simulation & Thermal Shock/Cycling
 - Upgraded Temperature and Measurement Capability from Original HATS System (160°C \rightarrow 260°C)
 - IPC-TM-650 Methods 2.6.27B & 2.6.7.2C
 - Replicate Temperature Conditions of Current Induced Heating Methodologies
 - Replicate any Convection Reflow Oven Surface Temperature Profile
 - Meet Current Automotive Reliability and Robustness Requirements
- The HATS^{2™} Tester Uses High-Speed "Air" as the Heat Transfer (Fluid) Mechanism
 - Temperature Range from -55°C to 260°C for Reflow Simulation & Thermal Cycling/Shock
 - Thermal Capacity to Transfer Test Coupon Core Temperature in 3-6 minutes (5-10 Cycles per hour)
 - 1000-Cycle Robustness or Reliability Testing Performed Within 1 Week
- Test Coupon Nets are Measured Using a 4-Wire System
 - High Current (up to 1A) allows Accurate Measurements to Micro-ohms
 - Test up to 72 (2-net) IPC-2221B "D" Coupons, 36 (4-net) Traditional HATS™ Coupons or 36 (7-net) HATS^{2™} Single Via Coupons*
 - Surface Temperature Measured Directly with Thermocouples





Introduction to HATS^{2™} Single Via Coupons*

- HATS^{2™} Single Via Coupon Uses Patented* Technology
 - Accurate, High Current, Micro-ohm Precision, 4-wire Resistance Measurement
 - 7 Single Vias and/or Daisy-chain Test Nets





- Why Single Vias Instead of Daisy Chains?
 - Daisy Chains can be Characterized as Resistors Connected in Series Circuit Via Circuit -
 - 50-90% of the Daisy Chain Resistance Comes from the Circuits Connecting the Vias Together
 - A 50% Separation/Crack in a Single Via Only Increases Daisy Chain Resistance Change by ~1%
 - In a Single Via Test this Change is Measured Directly as a 50% Change
 - Daisy Chains detect the end of Via(s) Failure while Single Via Testing Detects the Beginning of Via Failure

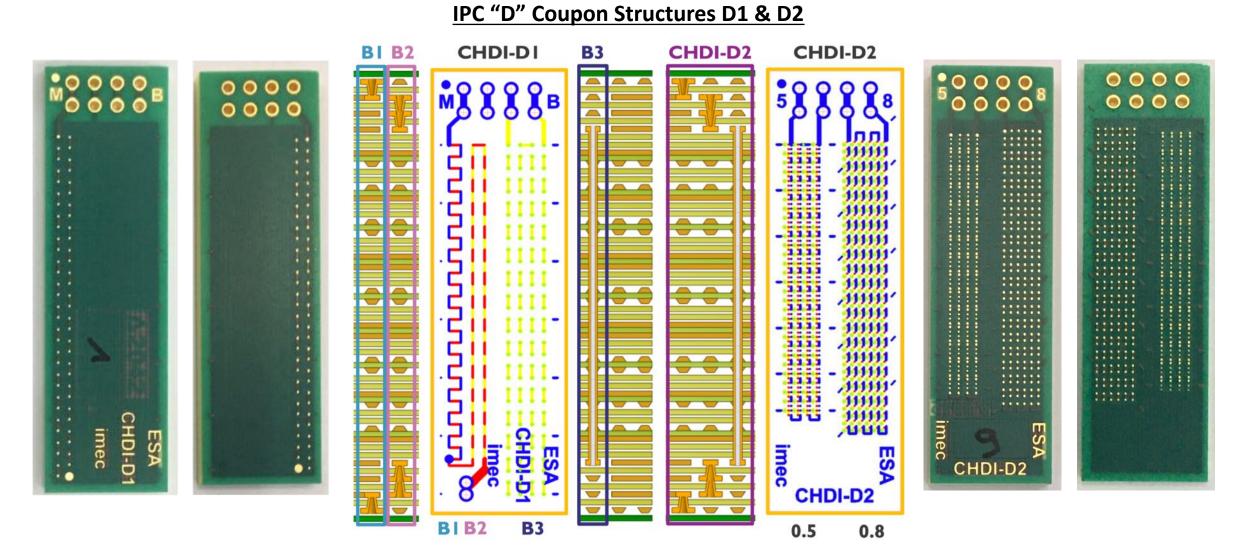


IPC/IMEC/ESA Microvia TV HATS² Test Program Goals

- Compare 6 Differing 3-Layer Stacked Microvia Structures to Each Other
 - Semi-Stacked Outside, Semi-Stacked Inside, Full Stacked, Full Staggered, Staggered Above Buried Via, Semi-Stacked Inside Above Buried Via Both on Top and Bottom of Test Coupon
 - Perform IPC-TM-650 Method 2.6.27B 230°C 6x Cycles of Reflow Simulation
 - Perform Subsequent Thermal Cycle Reliability and Robustness Testing (20% Change in Net Resistance Calculated as "Failure")
- Compare Results of "Reliability" Test (10°C Below T_g) to "Robustness" Test (20°C Above T_g)
 - "Reliability" Testing: 1000x Cycles from -55°C to 160°C
 - "Robustness" Testing: 500x Preconditioning Cycles from 25°C to 150°C followed by 1000x Cycles from 25°C to 190°C
- Compare IPC-2221 "D" Style Daisy Chain Coupons to HATS² Single Via Test Structures
- Compare a 1-Second Data Capture Interval to a 7-Second Data Capture Interval During IPC-TM-650 method 2.6.27B 230°C Reflow Simulation Testing



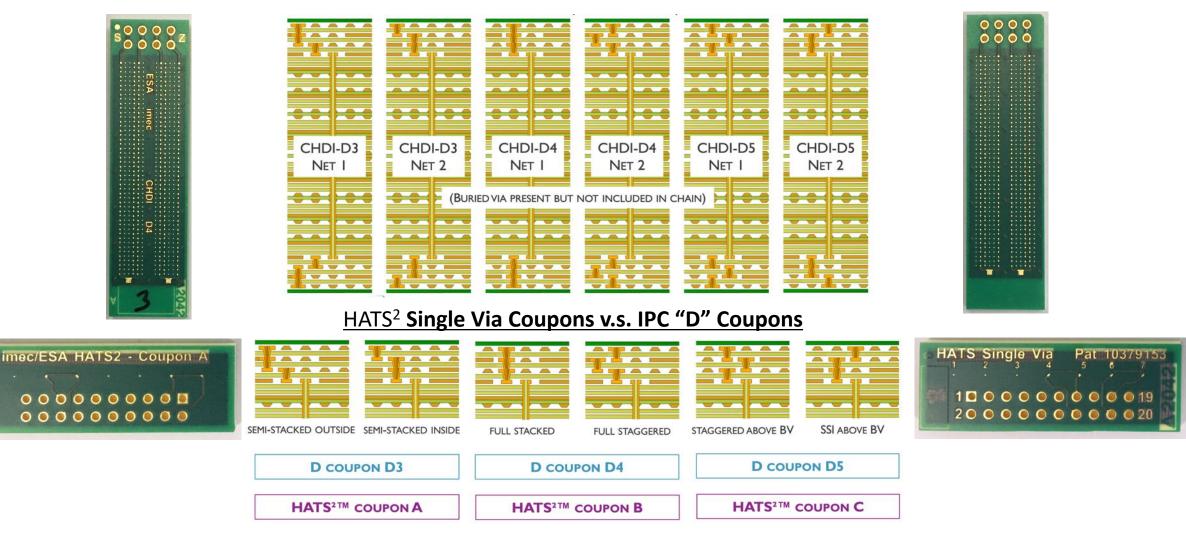
IPC/IMEC/ESA Microvia TV Structures Tested in HATS² Chamber





IPC/IMEC/ESA Microvia TV Structures Tested in HATS² Chamber

IPC "D" Coupon Structures D3, D4, D5 – Microvia Nets in Parallel on Either Side of Sample

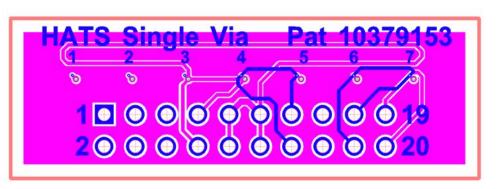




IPC/IMEC/ESA Microvia TV Structures Tested in HATS² Chamber

- HATS² Single Via Test Coupons* Contain 7 Test Nets that can be Single Vias or Daisy Chains
- HATS² Single Via Test Coupons Contain Circuitry that Allows Adjustments for Measurement and Temperature Drifts

HATS ² COUPON A		HATS ² CO	OUPON B	HATS ² COUPON C		
	SEMI-STACKED INSIDE	FULL STAGGERED	FULL STACKED	STAGGERED ABOVE BV	SSI ABOVE BV	
	I. MVs bottom		I. MVs bottom		I. MVs bottom	
2. MVs bottom		2. MVs bottom		2. MVs bottom		
3. Bur	ied via	3. Buried via		3. Buried via		
	4. Microvias top		4. Microvias top		4. Microvias top	
	5. MVs+BV+MVs		5. MVs+BV+MVs		5. MVs+BV+MVs	
6. MVs+BV+MVs		6. MVs+BV+MVs		6. MVs+BV+MVs		
7. Microvias top		7. Microvias top		7. Microvias top		



Net 1 & 4 are the same structure on the Top and Bottom of the Test Coupon

Net 2 & 7 are the same structure on the Top and Bottom of Test Coupon

Nets 5 includes a connected top to bottom via structure (microvias top, buried vias microvias bottom) Nets 6 includes a connected top to bottom via structure (microvias top, buried vias microvias bottom)

* U.S. Patent 10,379,153. German Patent 10 2019 006 553.0. Chinese Patent ZL 201922142627.1. Worldwide Patents Pending.

** images courtesy of imec



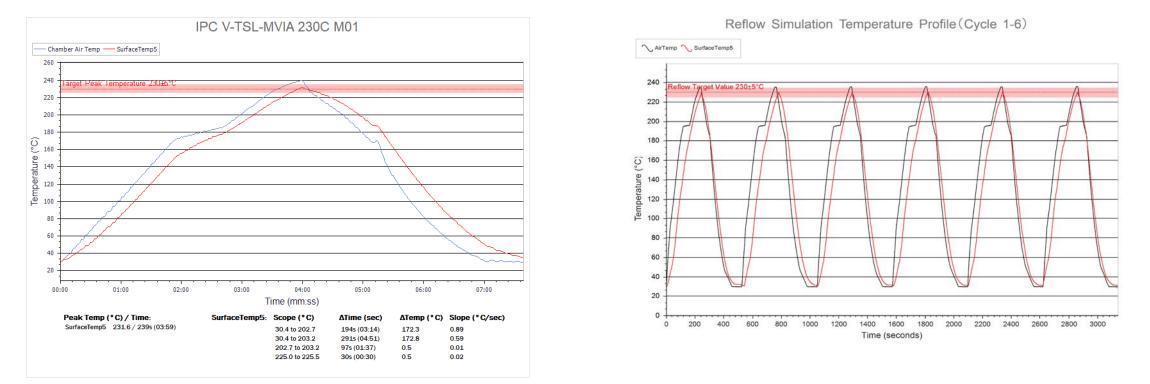
Results of Testing Program

- The Detailed Results of Testing are Contained in a 160+ Page Report
- Today I will Present a Highly Condensed Summary of the Test Results
- The Complete Test Report can be Downloaded at <u>www.HATS-Tester.com</u>
- The Samples were Tested in a HATS² Test System at Microtek Laboratories China
 - Samples were Logged In, Photographed and Labeled
 - A Small Area was Subjected to a Double TMA Test to Determine T_g (~170°C)
 - Reliability Test Temperature Range was then Set at -55°C to 160°C
 - Samples were Divided into Groups for Reliability and Robustness Exposures
 - All Samples in Test Plan were Exposed to IPC-TM-650 method 2.6.27B 230°C 6x Cycles of Reflow Simulation in the HATS² Test System
 - Samples Subjected to Reflow Simulation Were Subsequently Exposed to Reliability and Robustness Testing as Detailed in the Test Plan (see Complete Test Report for Details)



IPC-TM-650 Method 2.6.27B - 230°C 6x Cycles of Reflow Simulation

All Coupons in the Test Program were Subjected to 6X Cycles of IPC-TM-650 Method 2.6.27B - 230°C Reflow Simulation In the HATS² Tester Prior to Reliability and Robustness Testing

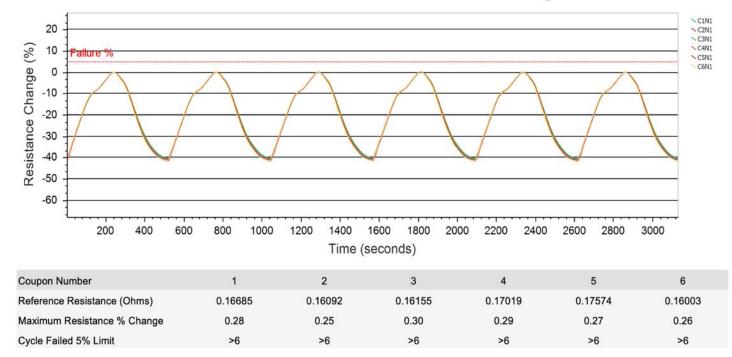


No Nets in Any of the Samples Failed During Reflow Simulation



IPC-TM-650 Method 2.6.27B - 230°C 6x Cycles of Reflow Simulation

- Typical Resistance Plot of IPC "D" Coupons 6 Coupons for Net 1
- Resistance at Reflow Peak Temperature 0.160 to .180 Ohms
- Change During 6 Cycles < 0.3%</p>

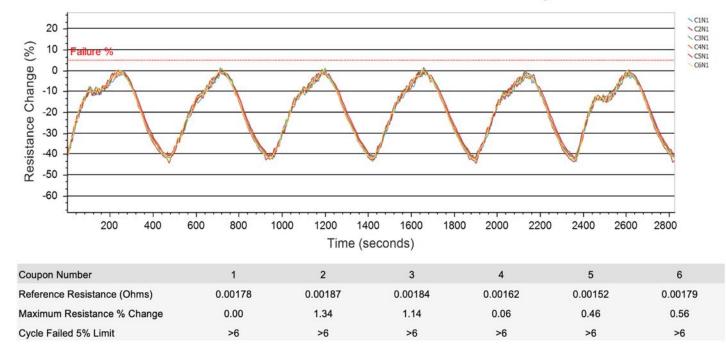


Reflow Simulation - Net 1 Resistance Change



IPC-TM-650 Method 2.6.27B - 230°C 6x Cycles of Reflow Simulation

- Typical Resistance Plot of HATS² Single Via Coupons 6 Coupons for Net 1
- Resistance at Reflow Peak Temperature 0.0015 to .0018 Ohms
- Change During 6 Cycles < 0.3%</p>



Reflow Simulation - Net 1 Resistance Change



IPC "D" Coupons – Daisy Chain with Micro Vias Only (No Buried Via)

- Each IPC-2221 "D" Coupon in Groups A3-B3, A4-B4 & A5-B5 Contained 2 Daisy Chain Via Nets Consisting of 288 Micro Vias on Both the Top and Bottom of the Coupon for Each of 2 Via Structures
 - The Micro Vias on the Top and Bottom of the Coupons in these Groups were Connected in Parallel by Design Without Buried Vias Included within the Net
 - Not a Typical "D" Coupon Design
 - Sensitivity of Each Net to Via Resistance Increases is Reduced by the Parallel Design
- 3 Types of Coupons Tested with 2 Micro Via Structures Per Coupon
 - Group "3" (Semi-Stacked Outside, Semi-Stacked Inside)
 - Group "4" (Full Stacked, Full Staggered)
 - Group "5" (Staggered Above Buried Via, Semi-Stacked Inside Above Buried Via)



IPC "D" Coupons – Daisy Chain with Micro Vias Only (No Buried Via)

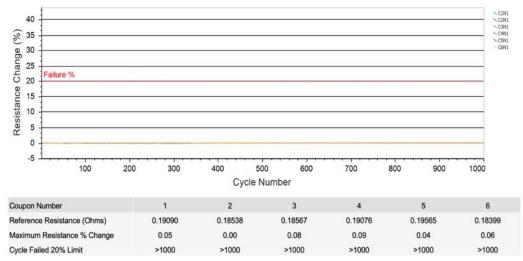
Typical Results of Reliability and Robustness Tests – Groups A3-B3, A5-B5

No Discernable Difference Between the Single Stacked Inside/Outside Structures

Group A3 Net 1 after -55°C to 160°C (1000x Cycles)

Cycle Range (°C): -55 to	160 Quality of Cycles: 1000	I	Failure Percentage (%	b): 20
Quantity of Coupons:	6 Number of Nets: 2	(Coupon Thickness:	2.8 mm
Net 1 Via Type: SS 0	utside (ParallelNet 1 Quantity of Holes:	288	Net 1 Hole Size: .12	25 mm
Net 2 Via Type: SS In	side (Parallel) Net 2 Quantity of Holes:	288	Net 2 Hole Size: .12	25 mm

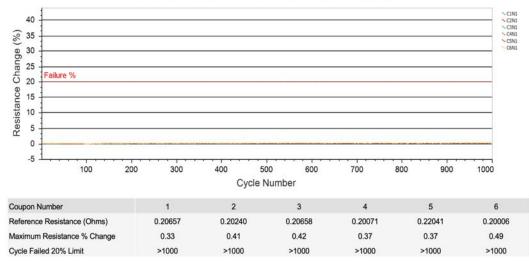
Thermal Cycling - Net 1 Resistance Change



Group B3 Net 1 after 25°C to 150°C (500x Cycles) Followed by Thermal Cycling 25°C to 190°C (1000x Cycles)

Cycle Range (°C): 25 to 150	/ 25 - 190	Quality of Cycles: 500/1000	Failure Percentage (%): 20
Quantity of Coupons:	6	Number of Nets: 2	Coupon Thickness: 2.8 mm
Net 1 Via Type: SS Outside	(Parallel)	Net 1 Quantity of Holes: 288	Net 1 Hole Size: .125 mm
Net 2 Via Type: SS Inside (F	Parallel)	Net 2 Quantity of Holes: 288	Net 2 Hole Size: .125 mm







IPC "D" Coupons – Daisy Chain with Micro Vias Only (No Buried Via)

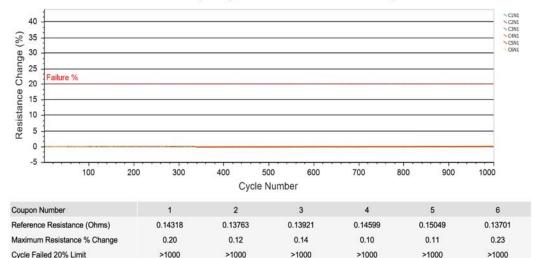
Typical Results of Reliability and Robustness Tests – Groups A4-B4

Coupon 3/6 - Net 1 (Full Stacked) Showed a Small Increase (1.5/3.5%) after Robustness Test

Group A4 Net 1 after -55°C to 160°C (1000x Cycles)

Cycle Range (°C)	: -55 to 160	Quality of Cycles: 1000		Failure Percentage	e (%): 20
Quantity of Coup	ons: 6	Number of Nets: 2		Coupon Thicknes	s: 2.8 mm
Net 1 Via Type:	Full Stacked (P	aralleNet 1 Quantity of Holes:	288	Net 1 Hole Size:	.125 mm
Net 2 Via Type:	Full Staggered	(ParaNel) 2 Quantity of Holes:	288	Net 2 Hole Size:	.125 mm

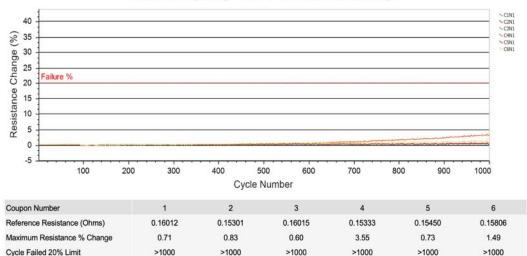
Thermal Cycling - Net 1 Resistance Change



Group B4 Net 1 after 25°C to 150°C (500x Cycles) Followed by Thermal Cycling 25°C to 190°C (1000x Cycles)

Cycle Range (°C): 25 to 150 / 25 to 190	Quality of Cycles: 500/1000	Failure Percentage (%): 20	
Quantity of Coupons: 6	Number of Nets: 2	Coupon Thickness: 2.8 mm	
Net 1 Via Type: Full Stacked (Parallel)	Net 1 Quantity of Holes: 288	Net 1 Hole Size: .125 mm	
Net 2 Via Type: Full Staggered (Parallel)	Net 2 Quantity of Holes: 288	Net 2 Hole Size: .125 mm	

Thermal Cycling - Net 1 Resistance Change





IPC "D" Coupons – Daisy Chain with Micro & Buried Vias

- The IPC "D" Daisy Chain Coupons (Test Groups C1-D1, C2-D2) were Only Subjected to Reliability Testing (-55°C to 160°C - 1000x Cycles)
- "Failure" Percentage was Set at 20%
- Group C1-D1 Contained 61 Buried Vias Only in Daisy Chain
- Group C2-D2 Contained 240 Single Stacked Inside, Micro Via Structures Integrated with Buried Vias in Daisy Chain
 - Net 1 was designed at 0.5 Grid
 - Net 2 was designed at 0.8 Grid
- The Results Did Not Show a Notable Difference Between the Two Grid Spacings
 - The Resistance was Higher for the 0.8 Grid Spacing as the Circuits Connecting the Via Structures were Longer Creating Increased Resistance
 - Percentage Differences Between the 2 Spacings will be Affected Differently by Similar Via Failures

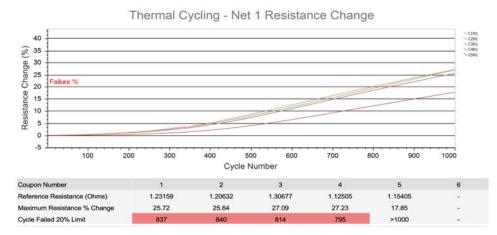


IPC "D" Coupons – Daisy Chain with Micro & Buried Vias

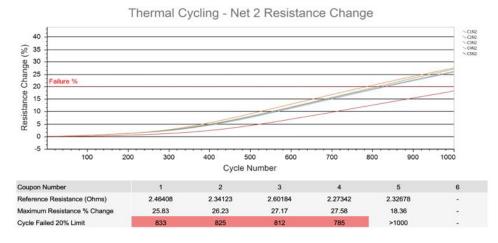
Group D1 Buried Via Net Thermal Cycling - Net 2 Resistance Change 40 C2N2 C3N2 C4N2 (% 35 eg 30 25 Failure % fu 20 15 10 500 100 200 300 400 600 700 800 900 1000 Cycle Number Coupon Number 2 4 3 Reference Resistance (Ohms) 0.74950 0.74410 0.72627 0.67587 0.81358 0.67729 Maximum Resistance % Change 54.14 48.47 41.84 52.95 40.41 40.21 Cycle Failed 20% Limit 479 563 585 479 508

Differences in Cycles to Failure Likely Due To Differences in Daisy Chain Resistance Affecting Percentage Contribution of Via Failure(s)

Group D2 Buried & SS Inside Via Net - 0.5 Grid



Group D2 Buried & SS Inside Via Net - 0.8 Grid





HATS² Single Via Coupons

- Each HATS² Single Via Coupon contains 7 Single Via Test Nets Consisting of:
 - 1 Single Via Net on Coupon Top Consisting of 1st Via Structure
 - 1 Single Via Net on Coupon Bottom Consisting of 1st Via Structure
 - 1 Single Via Net on Coupon Top Consisting of 2nd Via Structure
 - 1 Single Via Net on Coupon Bottom Consisting of 2nd Via Structure
 - 1 Single Via Net with Top and Bottom of 1st Via Structure Connected by a Buried Via
 - 1 Single Via Net with Top and Bottom of 2nd Via Structure Connected by a Buried Via
 - 1 Single Via Net Consisting of a Buried Via
- 3 Groups of Coupons Tested with 2 Micro Via Structures per Coupon.
 - Group "A" (Semi-Stacked Outside, Semi-Stacked Inside)
 - Group "B" (Full Stacked, Full Staggered)
 - Group "C" (Staggered Above Buried Via, Semi-Stacked Inside Above Buried Via)



HATS² Single Via Coupons – Isolated Via Structures

- Reliability Testing (10°C Below T_g): (Test Groups 1A-2A, 1B-2B, 1C-2C)
 - 1000x Cycles from -55°C to 160°C
- Robustness Testing (20°C Above T_g): (Test Groups 3A-4A, 3B-4B, 3C-4C)
 - 500x Preconditioning Cycles from 25°C to 150°C
 - 1000x Cycles from 25°C to 190°C
- Micro Via Structures Without Buried Vias Showed No Failures (<2% Actual Change) During Reliability Testing and Small Changes (<8% Actual Change) During Robustness Testing
 - The Semi-Stacked Outside & Semi-Stacked Inside Structures from Group 3A/4A Showed Increases of Resistance Between 2% and 4% after Robustness Testing
 - The Full Stacked Vias Structures from Groups 3B/4B Showed Increased Percentages
 Over the Semi-Stacked Via Structures After Robustness Testing (4%-8% vs. 1%-2%)



HATS² Single Via Coupons – Buried Vias

- Nets with Buried Via Structures Showed Failures in All Nets for Both Reliability and Robustness Testing
- Nets with Micro Via Structures that Included Buried Vias Showed Testing Failures in All Nets for Both Reliability and Robustness Testing
- "Full Staggered" and "Staggered Above Buried" Via Structures Demonstrated Increased Cycles to Failure in Both Reliability and Robustness Testing over other Micro Via Structures that Included Buried Vias
- The "Staggered Above Buried" Via Structure Showed the Highest Reliability of all the Via Structures with Buried Via included

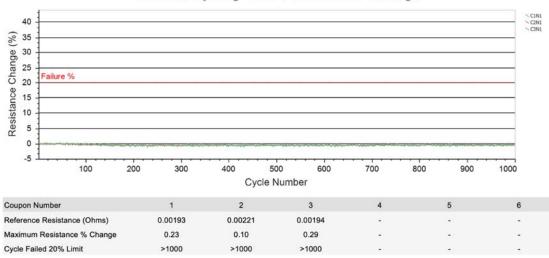


HATS² Single Via Coupons – Reliability Test Example

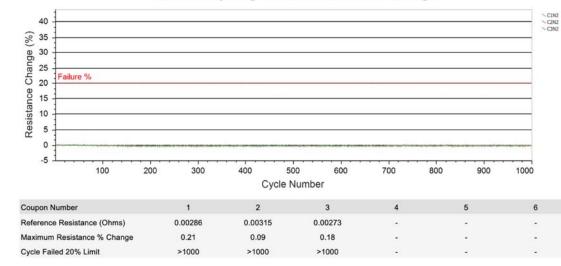
Group 2C, HATS² Single Via Coupons – Thermal Cycling -55°C to 160°C (1000x Cycles)

Cycle Range (°C): -55 to 160	Quality of Cycles: 1000	Failure Percentage (%): 20	
Quantity of Coupons: 3	Number of Nets: 7	Coupon Thickness: 2.75 mm	
Net 1 Via Type: SSI Above BV MV Bottom	Net 1 Quantity of Holes: 1	Net 1 Hole Size: .125 mm	
Net 2 Via Type: Staggered Above BV MV Bottom	Net 2 Quantity of Holes: 1	Net 2 Hole Size: .125 mm	
Net 3 Via Type: Buried	Net 3 Quantity of Holes: 1	Net 3 Hole Size: .25 mm	
Net 4 Via Type: SSI Above BV MV Top	Net 4 Quantity of Holes: 1	Net 4 Hole Size: .125 mm	
Net 5 Via Type: SSI Above BV MV+BV+MV	Net 5 Quantity of Holes: 1	Net 5 Hole Size: .125 mm	
Net 6 Via Type: Staggered Above BV MV+BV+MV	Net 6 Quantity of Holes: 1	Net 6 Hole Size: .125 mm	
Net 7 Via Type: Staggered Above BV MV Top	Net 7 Quantity of Holes: 1	Net 7 Hole Size: .125 mm	

Thermal Cycling - Net 1 Resistance Change



Thermal Cycling - Net 2 Resistance Change





C1N4

C2N4

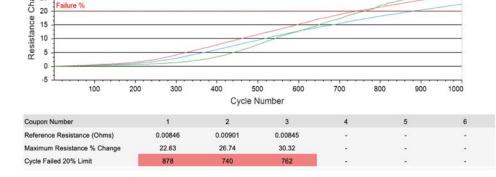
1000

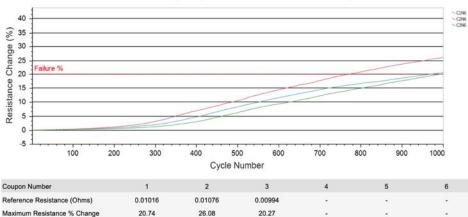
Results: HATS² Single Via Coupons – Reliability Test Example



Cycle Failed 20% Limit

965





989

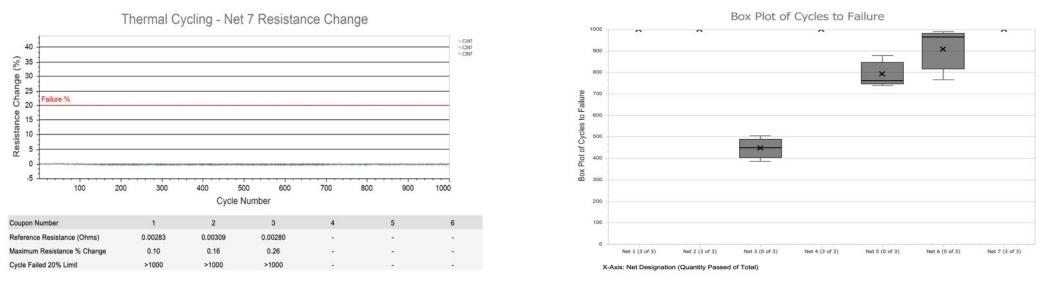
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25



HATS² Single Via Coupons – Reliability Test Example

Group 2C, HATS² Single Via Coupons – Thermal Cycling -55°C to 160°C (1000x Cycles)



- Net 5 (Staggered Above Buried Via) & Net 6 (Single Staggered Inside Above Buried Via) Lasted Longer than other Micro Via Structures Containing Buried Vias
- Net 6 (Single Staggered Inside Above Buried Via) Lasted Longest of Micro Via Structures that Included Buried Vias Although the Slightly Higher Via Resistance (~0.0001 Ohms at Peak) of Net 6 May Have Influenced the Contribution of the Failure to the Resistance Percentage
- Lower Cycles to Failure of Net 3 (Buried Via) Without Micro Via Structures is Expected as Net 5 & 6 Contain The Additional Resistance of Micro Via Structures which Decreases the Percentage Effect of the Resistance Caused by Buried Via Failure

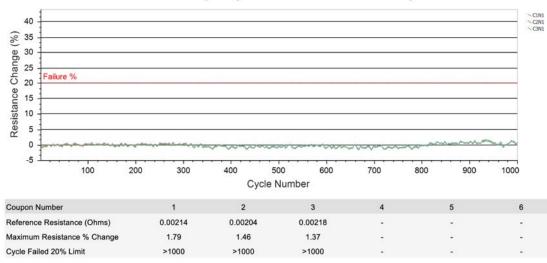


HATS² Single Via Coupons – Robustness Test Example

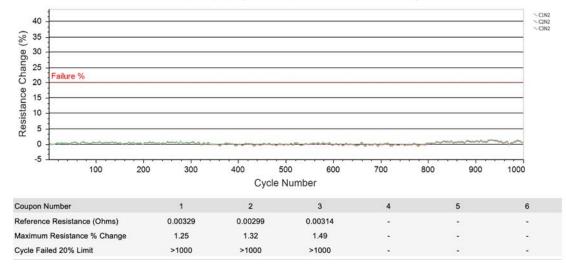
Group 4C, HATS² Single Via Coupons – Thermal Cycling Preconditioning, 25°C to 150°C (500x Cycles); Followed by Thermal Cycling 25°C to 190°C (1000x Cycles)

Cycle Range (°C): 25 to 150 / 25 to 190		Quality of Cycles: 500/1000	Failure Percentage (%): 20
Quantity of Cou	pons: 3	Number of Nets: 7	Coupon Thickness: 2.75 mm
Net 1 Via Type:	SSI Above BV MV Bottom	Net 1 Quantity of Holes: 1	Net 1 Hole Size: .125 mm
Net 2 Via Type:	Staggered Above BV MV Bottom	Net 2 Quantity of Holes: 1	Net 2 Hole Size: .125 mm
Net 3 Via Type:	Buried	Net 3 Quantity of Holes: 1	Net 3 Hole Size: .25 mm
Net 4 Via Type:	SSI Above BV MV Top	Net 4 Quantity of Holes: 1	Net 4 Hole Size: .125 mm
Net 5 Via Type:	SSI Above BV MV+BV+MV	Net 5 Quantity of Holes: 1	Net 5 Hole Size: .125 mm
Net 6 Via Type:	Staggered Above BV MV+BV+MV	Net 6 Quantity of Holes: 1	Net 6 Hole Size: .125 mm
Net 7 Via Type:	Staggered Above BV MV Top	Net 7 Quantity of Holes: 1	Net 7 Hole Size: .125 mm

Thermal Cycling - Net 1 Resistance Change



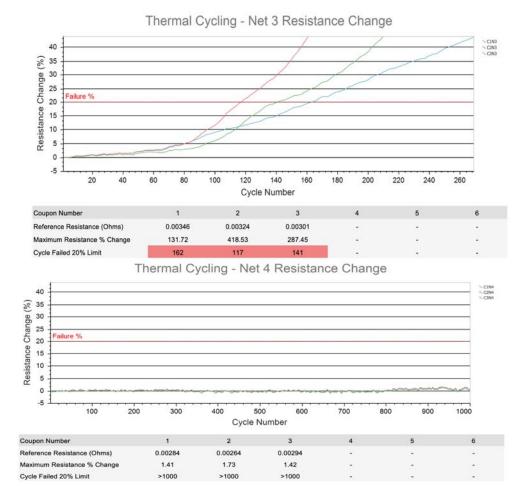
Thermal Cycling - Net 2 Resistance Change

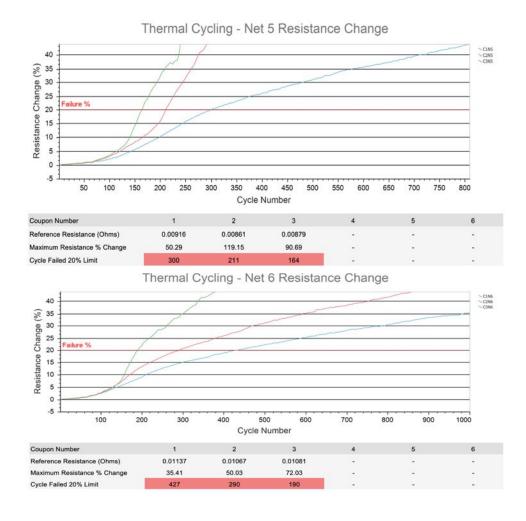




HATS² Single Via Coupons – Robustness Test Example

Group 4C, HATS² Single Via Coupons – Thermal Cycling Preconditioning, 25°C to 150°C (500x Cycles); Followed by Thermal Cycling 25°C to 190°C (1000x Cycles)

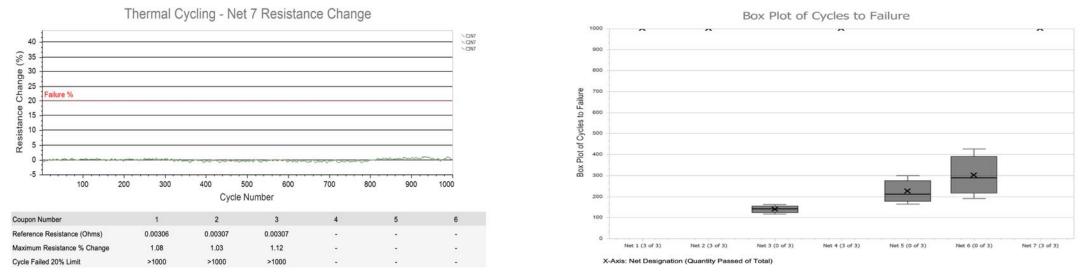






HATS² Single Via Coupons – Robustness Test Example

Group 4C, HATS² Single Via Coupons – Thermal Cycling Preconditioning, 25°C to 150°C (500x Cycles); Followed by Thermal Cycling 25°C to 190°C (1000x Cycles)



- Net 5 (Staggered Above Buried Via) & Net 6 (Single Staggered Inside Above Buried Via) Lasted Longer than other Micro Via Structures Containing Buried Vias
- Net 6 (Single Staggered Inside Above Buried Via) Lasted Longest of Micro Via Structures that Included Buried Vias
- Lower Cycles to Failure of Net 3 (Buried Via) Without Micro Via Structures is Expected as Net 5 & 6 Contain The Additional Resistance of Micro Via Structures which Decreases the Percentage Effect of the Resistance Caused by Buried Via Failure



Comparison of 1s to 7s Data Capture Interval During Reflow Simulation

- IPC-TM-650 Method 2.6.27B Currently Requires Data to be Acquired at 1-Second Intervals
- Periodic Monitoring is Intended to Capture Failure Events at or Near Peak Temperature

 Via Structures Can Fail at or Near Peak Temperature Then Reconnect as They Cool
- How Long of a Delay Between Data Points is Acceptable
 - 1s, 0.5s, 2s, 5s, 7s, 10s..... What's the Right Number?
 - 1s was Chosen Using Data and Capability from 1 System During Test Method Development
 - The HATS² System Became Available Late in the Method Development Process
 - We Submitted Data with 10-Second Data Acquisition Width and the Majority of Committee Members Voted to Keep 1-Second as the Test Method Requirement Based Upon Their Experience
 - Testing on the HATS² System has Shown that a 7-Second Data Acquisition Width is Adequate to Capture Failures at or Near Peak Reflow Temperature
 - 3-4 Data Points are Captured Within 5°C of Peak Reflow Temperature



Comparison of 1s to 7s Data Capture Interval During Reflow Simulation

- Why Does a 7-Second Data Capture Interval Make Sense?
 - Capacity of Samples for Simultaneous Testing
 - Measuring 24x IPC "D" Coupons Simultaneously Requires a Measurement System Capable of >50 Measurements / Second and can only be Accomplished with Digital Switches
 - Mechanical Switching Systems are Capable of Facillitating Accurate Low Resistance Values at ~20 Measurements Per Second (10x IPC "D" Coupons at One Time)
 - 7 Second Data Capture Intervals Would Allow Systems with High Current Mechanical Switching to Test as Many as 65 IPC "D" Coupons Simultaneously

Measurement Current – Low Resistance

- Digital Switching Systems are Capable of Very Fast Switching but Must Limit the Current of Measurement to <=10mA which in Turn Limits the Minimum Resolution of Resistance Measured to the 10s of Milliohms
- The Low Resistances of Single Via Testing (0.5 to 3 Milliohms) Require High Current in Order to Obtain Precise and Accurate Measurements
 - 0.1A for 0.010 to 0.100 ohm
 - 1A for resistances below 0.010 ohm
- Mechanical Switching Systems are Necessary for Measurement Current Above 10mA

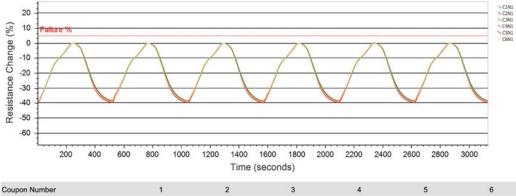


Comparison of 1s to 7s Data Capture Interval During Reflow Simulation

IPC 230°C Reflow Simulation Testing on "D" coupons

7 Second Between Measurements (Group C1)

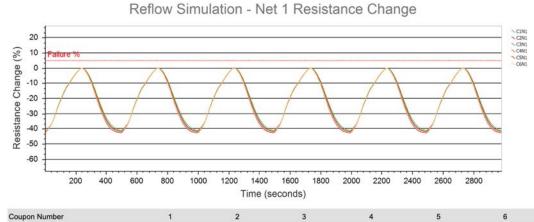




Coupon Number	1	2	3	4	5	D
Reference Resistance (Ohms)	0.24124	0.24260	0.27108	0.24459	0.23265	0.23811
Maximum Resistance % Change	0.12	0.12	0.04	0.06	0.22	0.06
Cycle Failed 5% Limit	>6	>6	>6	>6	>6	>6

4 Measurements within 5°C of Peak Temperature

1 Seconds Between Measurements (Group D1)



Coupon Number	1	2	3	4	5	6
Reference Resistance (Ohms)	0.24991	0.24259	0.23995	0.22123	0.24740	0.24548
Maximum Resistance % Change	0.22	0.21	0.26	0.20	0.21	0.22
Cycle Failed 5% Limit	>6	>6	>6	>6	>6	>6

29 Measurements within 5°C of Peak Temperature



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Ronson Sun Microtek Laboratories China www.TheTestLab.cn



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